

## Update on ROD Hardware and Test Status

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### **ROD status:**

- First Rev C boards distributed to pixel collaboration
- ROD and BOC passed SCT PRR in May at CERN
- New pixel-specific Rev E design is well-advanced

### **ROD testing status at LBL:**

- Progress using SimpleBOC and PP0 boards to test module
- Next steps

## Status of Rev C RODs

### Rev C ROD:

- First version of ROD with all major functionality operating correctly.
- Pixel collaboration to receive four of these RODs. One now in LBL, one in CERN (Bonn), and one in Genova. Final ROD for Wuppertal not sent yet.
- Have also begun sending SimpleBOC/PP0 boards. So far, one set in use in LBL, one sent to CERN, and third set in testing and almost ready for shipment to Genova.
- PP0 Support cards built and tested. Two in use in LBL (one in system test, one for ROD testing), one used at PS irradiation, one sent to CERN (Bonn), and one ready to ship to Genova shortly.
- Therefore, hardware for initial ROD software development is almost distributed.

### ROD + BOC underwent SCT PRR review in May at CERN:

- Review went well. Identified two major issues before production should be started. One was a recommendation to place Slave DSPs on mezzanine cards to allow future upgrade flexibility. The other was to ensure, as well as possible given schedule constraints, compatibility of SCT and Pixel designs. Also expressed concerns about calibration speed and optimization of histogramming.
- Presently have a Rev D design (all bug fixes applied to Rev C) waiting as a “backup” solution for SCT should there be problems with the new model.

## Towards a Production ROD: Rev E

### Rev E Design:

- In response to identified pixel concerns and SCT PRR concerns, a new, improved version is in the final phases of board layout.
- Two major items, discussed already last meeting:
- The size of the link FIFOs in the formatter FPGAs. We have insisted on a FIFO large enough to contain the largest data block which can be produced by the MCC.
- The available memory for the Slave DSP. We have presented an analysis suggesting that 256MB would be a better match to pixel histogramming needs than the present 32MB. This requires a change in DSP. Also implementing recommendation to place DSPs on a mezzanine card.
- Finally, as Xilinx parts families have evolved, much of the capability in the relatively expensive Virtex-E family is now available in the Spartan-II family. The footprints of the parts are different, but the cost is less than half. The VHDL does not need to change at all. All FPGA have now been switched to this new family, saving considerable money and allowing the larger link FIFOs requested by pixels.

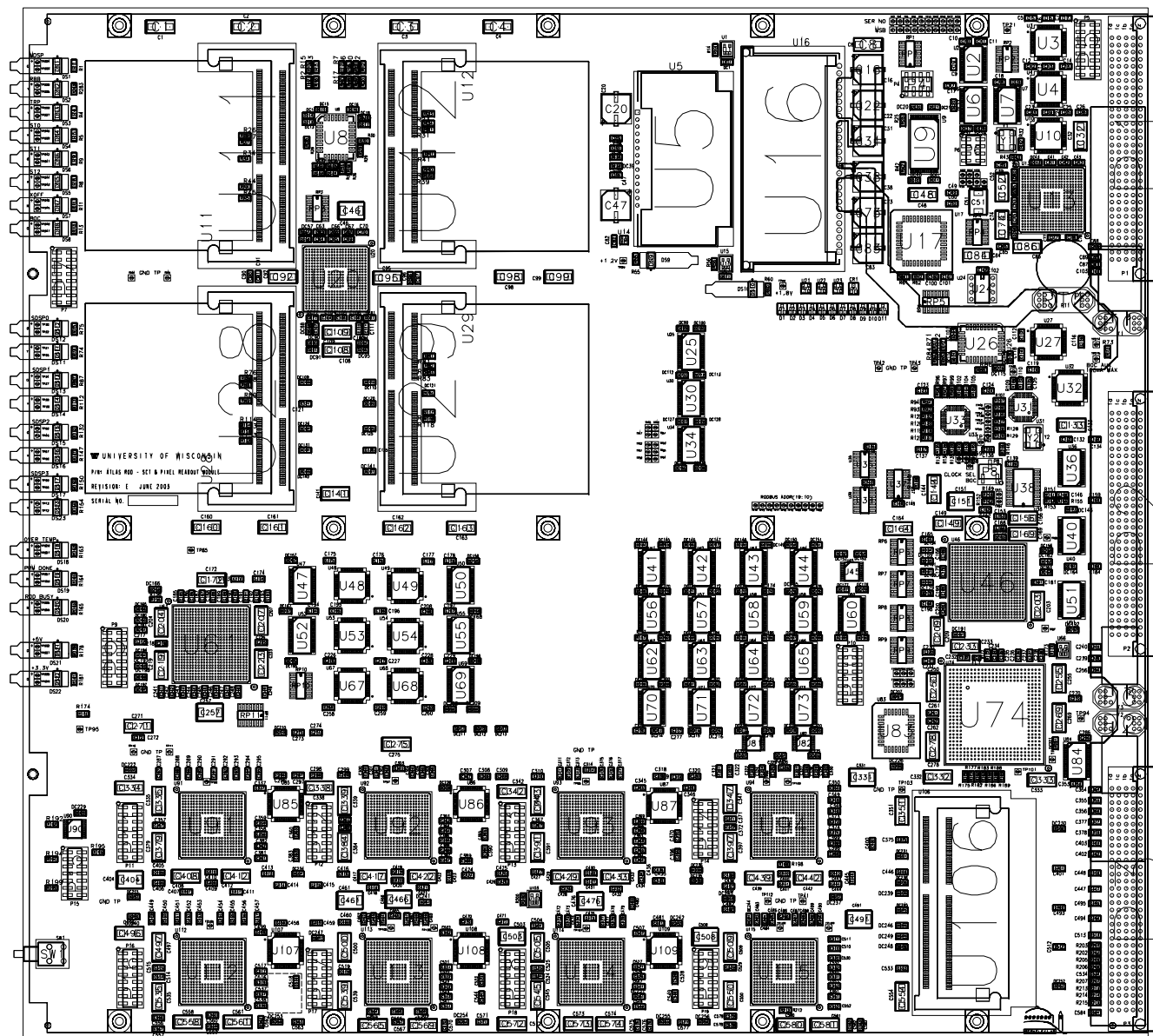
## Details:

- Have implemented a mezzanine card for new C6713 floating point DSP running at 200MHz (fastest clock rate compatible with 40MHz board clock). This board has a SIMM connector geometry, and includes 256MB of SDRAM. The size is roughly 6x6 cm.
- Spartan-II family of FPGA implemented. Formatters are 600E model, EFB is 400E model, Router is also 400E model.
- Debug memories (little used) have been dropped, and the board layout and bussing is much cleaner. Cypress PLL's have also been added to better manage the clock distribution to DSPs.
- Parts placement for main board and mezzanine board largely complete. Auto-routing underway, with anticipation of completion within about one week. Should lead to boards by about mid-July.
- Initially, will load two boards, one for pixels. Components ordered for 15 boards, so once first boards are working, more will follow rather quickly.

## Goals:

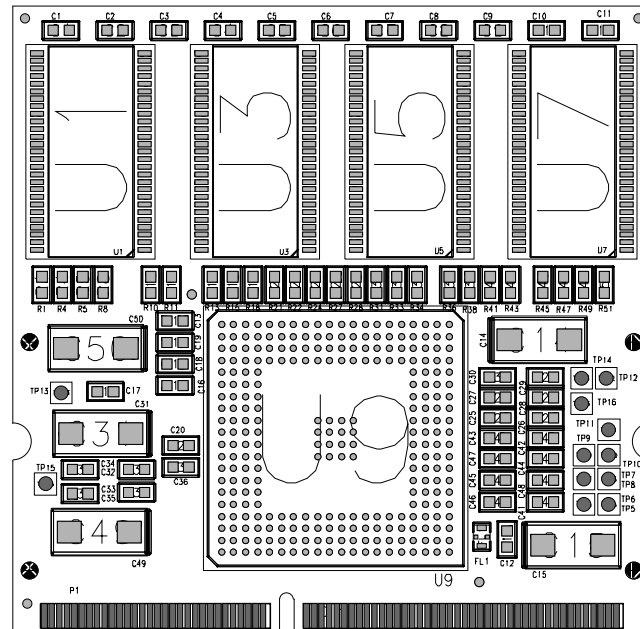
- Work to complete user evaluation for pixels this Fall.
- Aim to have PRR late this year and then proceed with production component orders.
- This requires that RODs cannot continue to get second priority to all other activities.

# Board layout for main board:



TOP SIDE SILKSCREEN TOP SIDE/SIGNAL 1 - LAYER 1  
+5V PLANE - LAYER 5  
SIGNAL 7 - LAYER 9  
GROUND PLANE - LAYER 3  
SIGNAL 4 - LAYER 6  
SIGNAL 8 - LAYER 10  
SIGNAL 2 - LAYER 3  
SIGNAL 6 - LAYER 7  
VCC PLANE - LAYER 11  
SIGNAL 3 - LAYER 4  
SIGNAL 5 - LAYER 8  
SIGNAL 9 - LAYER 12

# Board layout for mezzanine card:



TOP SIDE/SIGNAL 1 - LAYER 1

## **ROD Testing in LBL:**

- All work done with Rev C ROD and SimpleBOC cards. Work is a collaboration between John Richardson, and a student Joseph Virzi.
- Able to configure a pixel module from the TestStand using the official data structures.
- Able to read event data from Inmems, inject digital hits and get data routed back through Slave DSPs.
- No real analysis in DSPs, so data only verified by looking at dumps.
- Used existing SCT primitives as templates, and changed internal functions, plus added TestGlobal primitive.
- TestStand code modified to support pixel configuration files.

## Next Steps:

- Progress has slowed almost to a halt with irradiation and FE-I2 commitments.
- Pixlib on DSP is progressing.
- Still missing Pixel Register test support, and code for building scan masks.
- This should take less than two weeks to complete once JR is available.
- Histogramming for pixels in progress (Doug F. working on this), and trying to optimize speed through assembly coding and optimized data structures.
- Code which drives scans from DSP side is still needed.
- Working on calibration document to define all scans which should be implemented in ROD.
- Working on primitive document and additional pixel-specific primitives.
- Next major goal is to create a scan, which requires putting together many elements.

## Basic question:

- Should one continue to develop TestStand to include more TurboDAQ-like functions, as needed to support system testing, or should one concentrate on developing Paolo's DAQ-1 "pixlib" environment ?